

## CLAIMS

What is claimed is:

- 1 1. A content addressable memory (CAM) device comprising:
  - 2 a plurality of CAM cells;
  - 3 match lines coupled to respective rows of the CAM cells;
  - 4 storage circuits coupled to the match lines and configured to store, in response to assertion
  - 5 of a first timing signal, match indications signaled on the match lines; and
  - 6 a timing control circuit coupled to the storage circuits and configured to assert the first
  - 7 timing signal at either a first instant or a second instant according to the state of a
  - 8 mode select signal.
- 1 2. The CAM device of claim 1 wherein the timing control circuit receives a clock signal and a
- 2 first compare signal, and wherein the second instant occurs at least one cycle of the clock
- 3 signal after the first compare signal is asserted.
- 1 3. The CAM device of claim 2 wherein the first instant occurs prior to the second instant and
- 2 after the compare signal is asserted.
- 1 4. The CAM device of claim 2 wherein the second instant is substantially coincident with a
- 2 selected transition of the clock signal that occurs at least one cycle of the clock signal after
- 3 the first compare signal is asserted.
- 1 5. The CAM device of claim 4 wherein the selected transition of the clock signal follows a
- 2 first transition of the clock signal, the first transition of the clock signal occurring after the
- 3 first compare signal is asserted.

- 1       6. The CAM device of claim 5 wherein the first transition of the clock signal and the selected
- 2                  transition of the clock signal are both rising edge transitions of the clock signal.
- 1       7. The CAM device of claim 5 wherein the first instant occurs after the first transition of the
- 2                  clock signal and prior to the selected transition of the clock signal.
- 1       8. The CAM device of claim 7 wherein the timing control circuit comprises a delay circuit to
- 2                  enable assertion of the first timing signal after a delay interval following the first transition
- 3                  of the clock signal, the length of the delay interval determining the first instant.
- 1       9. The CAM device of claim 8 wherein the delay circuit includes a select input to receive a
- 2                  delay control value, the delay circuit being responsive to the delay control value to select
- 3                  one of a plurality of different time intervals to be the delay interval.
- 1       10. The CAM device of claim 9 further comprising a configuration circuit to store a value
- 2                  indicative of the delay control value.
- 1       11. The CAM device of claim 10 wherein the configuration circuit comprises a run-time
- 2                  programmable configuration register.
- 1       12. The CAM device of claim 10 wherein the configuration circuit comprises a storage
- 2                  location to store a value that controls the state of the mode select signal.
- 1       13. The CAM device of claim 1 further comprising an integrated circuit contact to receive a
- 2                  signal that controls the state of the mode select signal.

1       14. The CAM device of claim 1 wherein the second instant coincides with an edge of a clock  
2                  signal.

1       15. The CAM device of claim 1 wherein the timing control circuit comprises a delay circuit to  
2                  enable assertion of the first timing signal after a delay interval, the length of the delay  
3                  interval determining the first instant.

1       16. The CAM device of claim 15 wherein the delay circuit comprises a select circuit to select  
2                  one of a plurality of different time intervals to be the delay interval according to the state of  
3                  a delay control value.

1       17. The CAM device of claim 15 further comprising a one-shot circuit coupled to an output of  
2                  the delay circuit and configured to assert the timing control signal for a period of time after  
3                  the delay interval.

1       18. The CAM device of claim 1 wherein the timing control circuit comprises:  
2                  a first timing circuit to assert a first intermediate timing signal at the first instant;  
3                  a second timing circuit to assert a second intermediate timing signal at the second instant;  
4                  and  
5                  a select circuit to select, in response to the mode select signal, either the first intermediate  
6                  timing signal or the second intermediate timing signal to be the first timing signal.

1       19. The CAM device of claim 18 wherein the second timing circuit is configured to assert the  
2                  second intermediate timing signal at a time substantially coincident with a selected  
3                  transition of a clock signal.

- 1       20. The CAM device of claim 19 wherein the first timing circuit is configured to assert the first
- 2                  intermediate timing signal a delay time after a first transition of the clock signal, the first
- 3                  transition of the clock signal preceding the selected transition of the clock signal, and the
- 4                  delay time being less than the time interval between the first transition of the clock signal
- 5                  and the selected transition of the clock signal.
- 1       21. A content addressable memory (CAM) device comprising:
  - 2                  a CAM array to generate a plurality of match indications;
  - 3                  a configuration circuit to store a delay control value;
  - 4                  a timing control circuit coupled to receive the delay control value from the configuration
  - 5                  circuit and configured to generate a timing control signal a delay time after assertion
  - 6                  of a first control signal, the delay time being selected from one of a plurality of
  - 7                  different time intervals according to the delay control value; and
  - 8                  a storage circuit coupled to receive the match indications from the CAM array and
  - 9                  configured to store match indications in response to the timing control signal.
- 1       22. The CAM device of claim 21 wherein the configuration circuit is a run-time programmable
- 2                  storage register.
- 1       23. The CAM device of claim 22 wherein the configuration circuit comprises fused elements
- 2                  that are blown in a programming operation to store the delay control value.
- 1       24. A method of operation within a content addressable memory (CAM) device comprising:
  - 2                  generating a plurality of match indications in response to assertion of a compare signal; and
  - 3                  storing the plurality of match indications at either a first time or a second time according to

- 4                   the state of a mode select signal.
- 1       25. The method of claim 24 wherein generating a plurality of match indications in response to  
2                   assertion of a compare signal comprises asserting a compare enable signal in response to a  
3                   transition of a clock signal that occurs after assertion of the compare signal, the compare  
4                   enable signal enabling a comparand value to be output to an array of CAM cells within the  
5                   CAM device for comparison with contents thereof.
- 1       26. The method of claim 24 wherein storing the plurality of match indications at the second  
2                   time comprises storing the plurality of match indications substantially coincidentally with a  
3                   selected clock signal transition that follows assertion of the compare signal.
- 1       27. The method of claim 26 wherein storing the plurality of match indications substantially  
2                   coincidentally with a selected clock signal transition:  
3                   detecting a first transition of the clock signal that follows assertion of the compare signal;  
4                   detecting a second transition of the clock signal that follows the first transition of the clock  
5                   signal; and  
6                   storing the plurality of match indications in response to the second transition of the clock  
7                   signal.
- 1       28. The method of claim 27 wherein the first transition of the clock signal and the second  
2                   transition of the clock signal are both rising edge transitions of the clock signal.
- 1       29. The method of claim 27 wherein storing the match indications at the second time comprises  
2                   storing the plurality of match indications after the first transition of the clock signal and  
3                   prior to the second transition of the clock signal.

- 1       30. The method of claim 24 wherein storing the match indications at the second time comprises
- 2              delaying for a first time interval after assertion of the compare signal before storing the
- 3              match indications.
- 1       31. The method of claim 30 wherein delaying for a first time interval comprises delaying for a
- 2              time required for a timing signal to propagate through a delay circuit.
- 1       32. The method of claim 31 further comprising outputting a delay control value to the delay
- 2              circuit to select one of a plurality of different times required for the timing signal propagate
- 3              through the delay circuit.
- 1       33. The method of claim 32 further comprising storing the delay control value within a
- 2              configuration circuit of the CAM device.
- 1       34. The method of claim 33 wherein storing the delay control value within the configuration
- 2              circuit comprises issuing an instruction to a control circuit of the CAM device, the
- 3              instruction instructing the control circuit to store the delay control value within the
- 4              configuration circuit.
- 1       35. The method of claim 33 wherein storing the delay control value within a configuration
- 2              circuit of the CAM device comprises programming the delay control value within the
- 3              configuration circuit in a one-time programming operation.
- 1       36. The method of claim 35 wherein programming the delay control value within the
- 2              configuration circuit in a one-time programming operation comprises blowing one or more

3 fused elements within the CAM device.

1 37. The method of claim 24 wherein generating the plurality of match indications comprises  
2 generating signal levels on a plurality of match lines of the CAM device, and wherein  
3 storing the plurality of match indications at either a first time or a second time comprises  
4 asserting a detect signal at either the first time or the second time to enable a plurality of  
5 logic circuits to generate logic level outputs according to respective signal levels on the  
6 plurality of match lines.

1 38. The method of claim 37 wherein generating signal levels on a plurality of match lines of  
2 the CAM device comprises selectively discharging the match lines of the CAM device  
3 according to whether corresponding data words stored within the CAM device match a  
4 comparand value.

1 39. The method of claim 24 wherein storing the plurality of match indications at either a first  
2 time or a second time comprises generating a pulse at either the first time or the second  
3 time to enable a plurality of storage circuits to store the match indications.

1 40. The method of claim 24 wherein generating a pulse at either the first time or the second  
2 time to enable a plurality of storage circuits to store the match indications comprises  
3 asserting and then deasserting a latch enable signal to enable a plurality of latch circuits to  
4 store the match indications.

1 41. The method of claim 24 further comprising generating a match address that corresponds to  
2 a selected one of the match indications.

1       42. The method of claim 24 further comprising setting the mode select signal to a first state  
2                  during a wafer test of the CAM device and setting the mode select signal to a second state  
3                  during normal operation of the CAM device.

1       43. The method of claim 42 wherein setting the mode select signal to the first state comprises  
2                  contacting a contact point of the CAM device with a test probe.

1       44. A content addressable memory (CAM) device comprising:  
2                  means for generating a plurality of match indications in response to assertion of a compare  
3                  signal; and  
4                  means for storing the plurality of match indications at either a first time or a second, later  
5                  time according to the state of a mode select signal.

1       45. The CAM device of claim 44 wherein the means for storing the match indications at the  
2                  second time comprises means for storing the plurality of match indications after a first  
3                  transition of a clock signal and prior to a second transition of the clock signal.

1       46. The CAM device of claim 45 wherein the means for storing the match indications at the  
2                  first time comprises means for storing the plurality of match indications in response to the  
3                  second transition of the clock signal.